REMARKS

The application has been amended and is believed to be in condition for allowance.

The drawings were objected to for not illustrating the recited third and fourth current mirror circuits as claims in claims 6-8. Claims 6-8 were objected to as not accurately reciting the mirror circuit connections

Claim 6 has been amended to remedy the stated basis of objection.

With reference to Figure 2, there is illustrated an embodiment of the inventive differential amplifier.

See specification page 4 disclosing "The first differential amplifier section includes a first PMOS transistor which has a source connected with a power supply line, and a first pair of PMOS transistors which have sources connected with a drain of the first PMOS and gates respectively receiving first and second input voltages. The second differential amplifier section includes a first NMOS transistor which has a source connected with a ground line, and a second pair of NMOS transistors which have sources connected with a drain of the first NMOS and gates respectively receiving the first and second input voltages. The bias circuit activates one of the first and second differential amplifier sections in response to a control signal. The output circuit outputs an output signal from an output of the activated differential amplifier section."

Claim 1 recites that the differential amplifier circuit comprises first and second differential amplifier sections.

The first differential amplifier section is recited as comprising a first differential pair of PMOS transistors (11, 12) which receives first and second input voltages, respectively. The second differential amplifier section is recited as comprising a second differential pair of NMOS transistors (21, 22) which receive said first and second input voltages, respectively.

Claim 6 recites that the first differential amplifier section comprises a first current mirror circuit (44) whose input is connected with an output from one of said PMOS transistors (11) of said first differential pair and a second current mirror circuit (42) whose input is connected with an output from the other of said PMOS transistors (12) of said first differential pair.

Claim 6 also recites that the second differential amplifier section comprises a third current mirror circuit (41), one of whose outputs is connected with one of said NMOS transistors (21) of said second differential pair; and a fourth current mirror circuit (43), one of whose outputs is connected with the other of said NMOS transistors (22) of said second differential pair.

As to claim 7, see that the other output (drain of 41b) of said third current mirror circuit is connected with the input (gate of 42a) of said second current mirror circuit, and the other output (drain of 43b) of said fourth current mirror circuit is connected with the input (gate of 44b) of said first current mirror circuit.

Accordingly, Figure 2 is believed to illustrate the invention as recited in the amended claims. Withdrawal of the objections is solicited.

Claims 4, 5, 9-14, 19, and 20 were indicated to be directed to allowable subject matter.

In reliance thereupon, claims 4 and 9 have been amended to include the recitations of independent claim 1 and any intermediate claims.

Claims 4, 9, and 15 are therefore believed to be in condition for allowance, as well as their dependent claims. Allowance of claims 4-5, and 9-19 is therefore respectfully requested.

Claims 1-3, 6-8, and 15-18 were rejected as anticipated by HOJABRI 6,236,269.

Claims 1-2 and 15-16 were rejected as anticipated by HOGEBOOM 6,169,454.

Applicant respectfully disagrees.

The HOJABRI Reference

In the HOJABRI reference, a Rail-to-Rail circuit is realized by combining a differential stage for N-channel signals and a differential stage for P-channel signals. Both of the differential stage for N-channel signals and the differential stage for P-channel signals are biased at the same time.

On the other hand, in the present invention, one of the first transistor pair (P-channel differential stage) and the second transistor pair (N-channel differential stage) is selected, as described in claim 1. In the HOJABRI reference,

there is no description of the selection of the differential stage. Also, a switch circuit for the selection is not provided. Therefore, the HOJABRI reference cannot achieve the inventions of claims 1-3, and 15-18.

The HOGEBOOM reference

In the HOGEBOOM reference, the Rail-to-Rail circuit is realized by combining the differential stage for N-channel signals and the differential stage for P-channel signals. Also, like the HOJABRI reference, both of the differential stage for N-channel signals and the differential stage for P-channel signals are biased at the same time. However, the HOGEBOOM reference is different from the HOJABRI reference in that differential outputs are connected in common in parallel.

In the HOGEBOOM reference, there is no description of selection of one of the differential stages, like the HOJABRI reference. Therefore, the HOGEBOOM reference cannot achieve the inventions of claims 1, 2, 15, or 16.

Claim 1

As to HOJABRI, there are no first and second input voltages. The terms "first input voltage" and "second input voltage" must be given weight. There is only an input signal, Is. Although a differential voltage may be developed from the input signal, there are no first and second input voltages.

Accordingly, there is no disclosure of a first differential pair of PMOS transistors which receives first and

second input voltages, or a second differential pair of NMOS transistors which receive said first and second input voltages.

The input signal Is is not a control signal and the HOJABRI bias circuit does not activate one of the first and second differential amplifier sections in response to any control signal.

As to HOGEBOOM, there is no control signal. There is also no bias circuit which activates one of the first and second differential amplifier sections in response to any control signal. Note that transistors 40, 80 are gated from +Ve and -Ve supply and not controlled by any control signal.

Accordingly, claim 1 is believed novel.

Claim 2

As to HOGEBOOM, the Official Action has offered transistors 40, 80 as the first PMOS and first NMOS transistors, and has also offered transistors 40, 80 as the bias circuit.

But the recitation of claim 2 is that these first PMOS and first NMOS transistors are part of the first and second differential amplifier sections.

Therefore, the Official Action must acknowledge that either the recited bias circuit is missing or the first PMOS and first NMOS transistors of the amplifier sections are missing.

Also, column 5, lines 5-11 indicate that transistors 40, 80 are gate biased by fixed voltages through nodes 110, 115. This would indicate that there is no control signal and that this "bias circuit" does not stops an operation of the first PMOS transistor when activating the second differential amplifier

section, or stop an operation of the first NMOS transistor when activating the first differential amplifier section.

Thus, claim 2 is not anticipated.

Claim 7

HOGEBOOM M461, M463 are read by the Official Action as the recited fourth current mirror and M467, M38 as the first current mirror. Applicant does not see any "other output of said fourth current mirror circuit" connected with the input of said first current mirror circuit M467, M38.

The Method Claims

The Official Action acknowledges that the method claims are not explicitly disclosed. For the reasons outlined above, the claims are also not believed to be inherently disclosed.

Therefore, all the method claims are believed allowable.

New Claim 21

New claim 21 more specifically recites the disclosed structure.

Neither reference is seen as teaching or suggesting the recited combination of features found in claim 21.

More specifically the prior art does not teach or suggest i) gates of the differential pairs being connected to first and second input voltage terminals, ii) constant current sources connected to the differential pairs (as part of the differential amplifier sections), and iii) a control-signal

operated bias circuit stopping operation of one of the constant current sources when activating the other differential amplifier section.

Accordingly, new claim 21 is believed patentable.

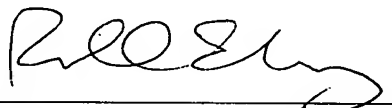
Taking the above into consideration, applicant believes the present application is in condition for allowance and an early indication of the same is respectfully requested.

Please charge the fee of $50 for the one extra dependent claim added herewith, to Deposit Account No. 25-0120.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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